EE 2700
Digital Circuits

Lab 8 – Sequence Finder

Objective: In this lab, the student will design and build a simple state machine, then use a debounced clock to debug it.

Preparation: Write the title and a short description of this lab in your lab book. Make sure the page is numbered and make an entry in the table of contents for this lab.

Design a state machine to find the sequence 110 in an incoming signal SIG. The machine should assert an output, FOUND (active low), when the sequence is found. The machine should start looking for the next sequence as soon as (a) the sequence is found or (b) a non-matching bit is detected. (The non-matching bit can be the start of a new sequence.) The design should use a 74LS74 Dual D flip-flop (make sure you have the pin diagram recorded before you start the lab). Test your design by simulating it with ISE and affix your simulation results to your lab book.

Note: The ISE library contains no flip-flop like a 74LS74, so create a file named ls74.vhd that contains the VHDL code given on the next page. Create a schematic symbol for it and use it in your design.

Design a de-bounce circuit using the single-pole double-throw switch, two resistors and two cross-coupled NAND gates. You will use this circuit to provide a clean clock that you can single-step to your state machine.

Connect FOUND and the state outputs (e.g. Q_1, Q_0) to LEDs as shown in Figure 1. This will enable you to see the output of the state machine and its current state.

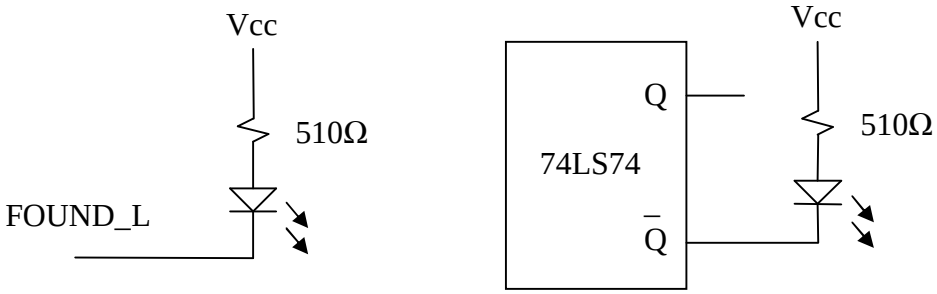

Figure 1 – LED Connections

Put a complete, labeled schematic in your lab book that includes the state machine, debounced clock, input switches and output LEDs. Completely

assemble your circuit on your proto-board and bring it, along with your lab book to the lab. Remember to initial and date each page.

Parts:
1 - 74LS74 (Dual D Flip-Flop)
1 - Single pole double throw switch for the CLK input
1 - DIP switch for the RESET(L) and SIG(H) inputs
3 - LEDs
3 - 510Ω resistors
Gates and inverters as needed.

Procedure: Use an oscilloscope to test your debounce circuit. Verify that both the rising and falling clock edges are clean (your lab instructor can help you with the oscilloscope).

Using the switches, input the following sequence to your state machine: 111**0**11**0**10011**0**011**0**. Verify the FOUND LED turns on when the zeros marked bold red are clocked into your circuit (and not at any other time).

Demonstrate to your lab instructor that your circuit detects the sequence 110 properly. (Your lab instructor may ask you to use a different input sequence than the one above.)

VHDL model for a 74LS74:

```
entity ls74 is
    Port ( CLK : in  STD_LOGIC;
           RST_L : in  STD_LOGIC;
           SET_L : in  STD_LOGIC;
           D : in  STD_LOGIC;
           Q_H : out  STD_LOGIC;
           Q_L : out  STD_LOGIC);
end ls74;

architecture Behavioral of ls74 is
begin

      process (CLK, RST_L, SET_L)
      begin
            if RST_L = '0' and SET_L = '0' then
                  Q_H <= 'X'; Q_L <= 'X';
            elsif RST_L = '0' then
                  Q_H <= '0'; Q_L <= '1';
            elsif SET_L = '0' then
                  Q_H <= '1'; Q_L <= '0';
            elsif CLK'event and CLK = '1' then
                  Q_H <= D; Q_L <= not D;
            end if;
      end process;

end Behavioral;
```

Signoff: A lab score can only be given if the circuit is functional.

Rubric (10 points total)

- Lab book is clearly legible and contains a title and description. (1 point)
- Lab book contains a state diagram (1 point)
- Lab book contains K-maps and logic equations for the next-state decoder and output decoder (1 point)
- Lab book contains a schematic with chips and pins labeled (1 point)
- Lab book contains simulation results (1 point)
- Lab book contains test results (1 point)
- Lab book contains a signed, dated summary (1 point)
- Each used page has a page number and is initialed* and dated* with no obliterations (1 point)
- The circuit is functional before the end of the lab period. (2 points)

Note: If the circuit is working at the end of the lab period but the lab book is not yet complete, the lab can be signed off as “working”, and no late penalty will be assessed if it is graded on or before the next lab period.

* It is not necessary to initial and date a page that contains a signature and date unless the dates are different.